

WHAT IS CLAIMED IS:

1 1. A bipolar transistor, comprising:
2 a substrate;
3 a semiconductor intrinsic base layer formed by blanket epitaxy on the
4 substrate;
5 a collector layer formed on the substrate;
6 an emitter formed over the semiconductor intrinsic base layer, forming a
7 junction between the semiconductor intrinsic base layer and the emitter, wherein the junction
8 at a lateral portion of the emitter extends farther into the intrinsic base layer than the junction
9 at a center portion of the emitter;
10 an extrinsic base formed adjacent to the lateral portion of the emitter;
11 a base electrode formed on a portion of the extrinsic base layer;
12 a collector electrode formed on a portion of the collector layer; and
13 an emitter electrode formed on a portion of the emitter layer.

1 2. A bipolar transistor as claimed in claim 1, wherein the emitter comprises a
2 pedestal having a top which contacts an emitter layer.

1 3. A bipolar transistor as recited in claim 1, wherein a raised extrinsic base layer
2 is formed and comprises one of a highly-doped polysilicon or a highly-doped amorphous

3 silicon.

1 4. A transistor as recited in claim 1, wherein the lateral portion has a depth in
2 a range of approximately 20-40 nm.

1 5. A bipolar transistor as recited in claim 1, wherein the semiconductor intrinsic
2 base layer comprises silicon germanium.

1 6. A bipolar transistor as recited in claim 1, further comprising a sidewall spacer
2 formed between and electrically isolating the emitter and the extrinsic base layer.

1 7. A bipolar transistor as recited in claim 6, wherein the sidewall spacer
2 comprises one of a silicon nitride, a silicon dioxide, or a combination of the two.

1 8. A bipolar transistor as recited in claim 7, wherein the sidewall spacer has a
2 width in the range of 10 to 70 nanometers.

1 9. A bipolar transistor as recited in claim 2, wherein the emitter comprises one
2 of a polysilicon or an amorphous silicon.

1 10. A bipolar transistor as recited in claim 1, wherein the emitter layer has a
2 thickness in the range of 30 to 200 nanometers.

1 11. A bipolar transistor as recited in claim 1, wherein the emitter is in-situ doped
2 with phosphorous that minimizes drive-in and activation anneal temperatures.

1 12. A method of making a bipolar transistor, comprising:
2 providing a semiconductor intrinsic base layer on a substrate;
3 providing a collector layer on the substrate;
4 providing a semiconductor intrinsic base layer on the substrate;
5 providing a mandrel or removable region in the location of an emitter;
6 providing a recess adjacent to mandrel films into the semiconductor intrinsic
7 base layer to form a silicon pedestal;
8 providing an insulating spacer adjacent to the silicon pedestal and mandrel
9 films;
10 providing an emitter on the semiconductor intrinsic base layer which contacts
11 the intrinsic base layer in the former location of the mandrel films and which extends a
12 distance wider than the silicon pedestal and a distance below a top surface of the silicon
13 pedestal, the semiconductor intrinsic base layer forming a junction with the emitter;
14 providing a base electrode on a portion of raised extrinsic base layer;
15 providing a collector electrode on a portion of the collector layer; and
16 providing an emitter electrode on a portion of the emitter layer.

1 13. A method of making a bipolar transistor as recited in claim 13, wherein the

2 recess has a thickness in the range of 5 to 50 nanometers.

1 14. A method of making a bipolar transistor as recited in claim 13, wherein a
2 raised extrinsic base layer is formed and comprises one of a highly-doped polysilicon or a
3 highly-doped amorphous silicon.

1 15. A method of making a bipolar transistor as recited in claim 13, wherein the
2 bipolar transistor is a heterojunction bipolar transistor.

1 16. A method of making a bipolar transistor as recited in claim 13, wherein the
2 semiconductor intrinsic base layer comprises silicon germanium.

1 17. A method of making a bipolar transistor as recited in claim 13, wherein a
2 sidewall spacer formed between and electrically isolating the emitter layer and the extrinsic
3 base layer.

1 18. A method of making a bipolar transistor as recited in claim 17, wherein one
2 of a silicon nitride, a silicon dioxide, or a combination of the two is used for the sidewall
3 spacer.

1 19. A method of making a heterojunction bipolar transistor as recited in claim 17,
2 wherein the sidewall spacer is provided with a width in the range of 10 to 70 nanometers.

1 20. A method of making a heterojunction bipolar transistor as recited in claim 13,
2 wherein one of a polysilicon or an amorphous silicon is used for the emitter layer.

1 21. A method of making a heterojunction bipolar transistor as recited in claim 13,
2 wherein the emitter layer is provided with a thickness in the range of 30 to 200 nanometers.

1 22. A method of making a heterojunction bipolar transistor as recited in claim 13,
2 further comprising in-situ doping the emitter layer with phosphorous to minimize drive-in
3 and activation anneal temperatures.